Electronic Version
Stylesheet Version v1.1.1

Memory Module with Dynamic Termination Using Bus Switches Timed by Memory Clock and Chip Select

Abstract

A low-power memory module has an active termination circuit at each end of critical signal traces. The dynamic termination circuit has a low-value resistor that is connected to a termination voltage by a transmission gate that is turned on by a switch signal. The switch signal is activated when the memory module is selected by a chip-select signal, and when a time window is open. The time window is generated from the clock to synchronous DRAMs on the memory module. The time window can be one-quarter of the clock period by ANDing the clock and a delayed clock that is delayed by one-quarter of a cycle. A static terminating resistor in parallel with the low-value resistor provides a much smaller terminating current that is not switched on and off. Traces can be impedance-matched at junctions to branches that each has a dynamic termination circuit at the far end.